REMARKS

The examiner has maintained the rejections that were made in the prior office action and has made the rejection final. The applicant hereby requests that the rejections be reconsidered and withdrawn in light of the comments below and in view of the attached documentary exhibits.

Applicants understand from the Final Action that the Examiner maintains his position that the invention as claimed is obvious over DE 195 45 231 A1 (DE `231) and optionally in view of Landau (U.S. Pat. No. 6,261,433) or over Ritzdorf et al. (US 2002/0074233 A1) in view of either Schumacher et al. (U.S. Pat. No. 5,976,341) or DE 43 44 387 A1 (DE `387).

The arguments of the Examiner are as follows:

DE `231 differs from the claimed invention because it does not disclose that the substrate can be a semiconductor substrate and that it would hence have been obvious to one having ordinary skill in the art at the time the invention was made to have used a semiconductor substrate in place of the circuit board disclosed by DE `231 because semiconductor substrates and circuit board substrates have equivalent properties. Further, since the actual method of electroplating occurs on the basic metal layer, one skilled in the art would recognize that the actual substrate would be irrelevant, *i.e.* the substrate could be any material, because the effective substrate on which the copper layer is plated would be the conductive basic layer. Furthermore, the prior art would have recognised that electroplating on semiconductors would be equivalent to electroplating on printed circuit boards (PCBs), as would be apparent from Landau.

As an additional grounds for rejecting the claims the Examiner cites Ritzdorf et al. to show a method of electroplating copper specifically applied to semiconductor wafers. the Examiner states that with respect to the claimed invention the method of Ritzdorf et al. differs by not disclosing an Fe(II) compound or Fe(III) compound in the copper deposition bath. The

Examiner goes on to state that it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Ritzdorf et al. to use iron compounds and copper parts to generate copper ions as taught by Schumacher et al. and in DE `387 because the iron compounds and copper parts provide the copper necessary for plating copper when inert anodes are used.

According to the Examiner's opinion the applicant's arguments have not considered persuasive because no evidence has been provided to support the statement that Fe(II) and Fe(III) are a semiconductor poison. Further the electrolytic deposition would plate copper layers on the basic metal layer. The electrolytic solution would therefore never come into contact with the semiconductor. As a consequence the actual method steps might be used to plate any substrate that has a full-surface basic metal layer coating the substrate.

In response the applicants state as follows:

In all of the art cited by the Examiner if the disclosed electroplating method is intended for metallizing wafers then the electroplating liquid does not contain Fe(II) and/or Fe(III), and if the electroplating liquid does contain Fe(II) and/or Fe(III) then the disclosed method invariably is intended for use in PCB production and not for semiconductor processing, *e.g.* consider Ritzdorf et al. and DE `231. This clear trend in the prior art demonstrates that there was a prejudice against the use of iron in processes for manufacturing integrated semiconductor circuits at the time the invention was made.

This prejudice against the use of iron in processes for manufacturing integrated semiconductor circuits is conclusively demonstrated by the attached specifications and papers designated as Exhibits A through D. These exhibits include:

(1) SEMI specifications (Exhibit A)

(2) Byoung-Deog Choi et al. in: Jpn. J. Appl. Phys., Vol. 40, pp. L915 - L917 (Exhibit B)

(3) A.A. Istratov et al. in: Appl. Phys. A 69, pp. 13 - 44 (Exhibit C)

(4) A.A. Istratov et al. in: Appl. Physics A 70, 489 - 534 (Exhibit D)

As to item (1):

SEMI is an abbreviation for the SEMICONDUCTOR ENGINEERING AND MANUFACTURING INSTITUTE, which has issued specifications for the silicon devices used in chip manufacturing processes and for the chemicals used in these manufacturing processes. The specifications for the permissible iron content in silicon wafer material outlined in the SEMI specifications are extremely low so that those skilled in the art have known that suitable measures have to be taken to practically completely prevent iron from diffusing into the silicon wafer. Accordingly, even trace amounts of iron have to be prevented from coming into contact with the wafer.

The SEMI specification sets the tolerable limits for the presence of certain species in the semiconductor manufacturing processes or in semiconductor wafers, these limits varying depending on the calendar year (starting with 1999 and ending up with 2005). Referring to the liquid chemicals used in processing the wafers, apart from copper only iron is cited as the specific critical metal impurity in Table 80a. The concentration of these two species in the chemicals (HF, H_2O_2, NH_4OH) must each be below 250 ppt (parts per trillion) in 1999 and must each be below 100 ppt in 2005. According to another Table the concentration limits for iron are somewhat higher and range from 5 ppb maximum (for nitric acid [SEMI specification C35-0301]) to 2.0 ppm (for grade 1 phosphoric acid [SEMI specification C36-0301]). Furthermore total bulk iron in the silicon wafer material must be below 10^{10} atoms cm^{-3} (Table 32a) which

level corresponds to a concentration of about $1 \cdot 10^{-13}$ g Fe cm^{-3} (equal to 0.1 pg cm^{-3}; as a comparison a calculation in exhibit D shows that if an iron contamination level of 10^{11} atoms cm^{-3} is to be achieved in the whole yearly world production of silicon, then the total mass of iron in the whole yearly world production of silicon cannot exceed 10 mg! [page 520, left col., 26th – 28th line]). Those skilled in the art would readily recognise that such low concentrations can extremely quickly accumulate even by unintentional contamination from sources commonly encountered in semiconductor manufacturing. As to the surface concentration of iron atoms on silicon surfaces the maximum tolerable limit was set to $9 \cdot 10^{8}$ atoms cm^{-3} in 1999 and to $2.5 \cdot 10^{8}$ atoms cm^{-3} in 2005 (Table 82a).

It is clearly seen from the above that iron has been considered an extremely critical contaminant element in semiconductor manufacturing and hence a "semiconductor poison" as stated as previously stated by the applicants.

In reference to Exhibit B:

A theoretical and experimental report of the effects that iron atoms and iron ions have in silicon wafers has been given by Byoung-Deog Choi et al and is attached hereto as exhibit B. According to their study the tolerable iron content in a silicon wafer is even lower level than was expected before because of so-called "latent" iron that could not be detected easily below a level of $4.5 \cdot 10^{12}$ atoms cm^{-3} (page L915, left col., 7th – 5th from the last line). The authors of this study have also reported that the International Roadmap for Semiconductors would require a level for iron in silicon wafers that would be lower than 10^{10} atoms cm^{-3} (page L915, left col., 4th – 6th line). This corresponds to the extremely low levels of iron noted previously, which can be tolerated in semiconductor processing.

Further Byoung-Deog Choi et al. report that iron is critical for today's silicon, "since such device parameters as diode leakage current, gate oxide integrity, and carrier lifetime depend strongly on iron density" (page L915, left col., 19^{th} – 22^{nd} line). It is because of these reasons that iron is considered a "semiconductor poison" as was stated previously.

The authors refer to the experimental result that iron forms ion pairs with boron in silicon, which has been doped with boron.

In reference to Exhibits C and D:

Exhibit C represents the first part of a series of two review articles which impressively demonstrate the importance attributed to iron by those skilled in the field of semiconductor processing. To begin with, the authors of this review have focussed on reviewing the properties of iron in silicon because "iron is one of the most ubiquitous and detrimental metal impurities in silicon" (emphasis ours; exhibit C, page 13, paragraph bridging the left and right columns). "Since the ultrapure technology that enables one to reduce iron surface contamination to the level of below 10^{10} to 10^{11} cm^{-2} is extremely expensive, it has become increasingly important to understand the mechanisms of iron contamination, the detrimental role of iron in silicon devices, and the tolerable limits of iron contamination for each particular technological process. This demand has stimulated great interest in the physics of iron in silicon". Therefore, iron is clearly a detrimental contaminant in silicon, the concentration of which those skilled in the art go to extreme expense in order to reduce as much as possible.

Similar statements are made in Exhibit D. "The Semiconductor Industry Association (SIA) International Technology Roadmap specifies $1.4 \cdot 10^{10}$ cm^{-2} as the maximum allowable surface iron contamination in the year 2000, decreasing to $5 \cdot 10^{9}$ cm^{-2} of iron in 2005." (See page 489, sentence bridging the left and right columns). "Iron is certainly one of the most

troublesome contaminants in the IC industry. Iron is a very common element in nature, and is difficult to completely eliminate on a production line." (See page 489, right col., $5^{th} - 8^{th}$ line). In lines 10 and 11 the detrimental role of iron in silicon devices is specifically described. The extreme requirements for low concentrations of iron in silicon wafers is also evident from the study of Schmidt et al. as reported by A. A. Istratov et al. in Exhibit D (page 492, left col., $7^{th} - 4^{th}$ from the last line), who found that, "one can introduce about $2 \cdot 10^{13}$ cm^{-3} of Fe in a 3-inch silicon wafer just by lifting it repeatedly with metal tweezers!"

Similar to Byoung-Deog Choi et al. A. A. Istratov et al. describe the detrimental behaviour of iron in semiconductor processing (Exhibit D, page 489, $12^{th} - 26^{th}$ line), which includes:

i) introducing deep levels in the band gap, reducing the minority carrier lifetime, or generating minority carriers in depleted regions,

ii) incorporation of iron into the gate oxides, or degrading MOS device yield by precipitation of iron at Si/SiO_2 interfaces,

iii) very high diffusion coefficients at high processing temperatures resulting in fast contamination of large wafer areas even from point sources and from the wafer backside,

iv) forming precipitates or complexes that deleteriously affect the device yield, which is due to the steep temperature dependence of the solubility of iron in silicon, which in turn results in silicon becoming supersaturated with iron during cooling even at relatively low iron concentrations, and

v) the relatively high diffusivity of iron even at low temperatures facilitating the defect reactions involving supersaturated iron.

From the above it will be apparent that those skilled in the field of semiconductor processing have been aware of the detrimental behaviour of iron and of the extreme danger posed by even trace amounts of iron to the proper functioning of semiconductor devices. Therefore those skilled in the art have undertaken and still undertake great efforts to study the behaviour of iron in silicon and its impact on the functionality of silicon devices, to further develop analytical tools for verifying that the iron concentrations in silicon wafers is in compliance with the very low acceptable values, and to study how to further reduce the concentration of iron in silicon wafers and mitigate the detrimental effects of the existing iron. Therefore, it should be readily apparent from the attached exhibits that those skilled in the field would have a very strong aversion to exposing silicon wafers and devices to electroplating solutions that contain Fe(II) and/or Fe(III) ions because of the expected negative impact thereof on the functionality of the silicon devices. Those skilled in this field would therefore never have seriously considered the application of such electroplating solutions to silicon wafers and devices and from the very first moment would have and indeed have rejected this idea.

The Examiner based his finding that our previously submitted arguments were unpersuasive on the observation that the wafers that are to be electroplated are coated with a conductive base coat. Based on this observation the Examiner concludes that the electrolytic solution would never come into contact with the semiconductor material of the wafer and therefore one of ordinary skill in the art would not see any obstacle to the immersion of wafers coated with the conductive base coat in the electroplating solutions that contain Fe(II) and/or Fe(III) ions. Although such an argument may at first seem reasonable, this argument completely ignores the very real process of solid state diffusion of which those of ordinary skill in the art are keenly aware.

The fact that iron containing baths are used to electroplate PCBs is no guarantee that the same baths can be used to electroplate semiconductor wafers without adversely impacting the function of the active circuit elements formed in the wafer. The PCB substrate is inert and serves no purpose other than to provide an insulating mechanical support. The semiconductor wafer on the other hand has formed within it active circuit elements such as diodes and transistors whose proper functioning is intricately bound to the physical condition and nature of the semiconductor wafer. Any alteration of the physical nature of the semiconductor wafer by, for example, the diffusion of a detrimental impurity such as iron into the wafer, will very likely adversely impact or destroy the functioning of the active circuit elements formed in the wafer. In establishing a *prima facie* case of obviousness the Examiner bears the burden of showing a reasonable basis in the prior art to expect not just that the electroplating methods used with PCBs can be used to electroplate a semiconductor wafer substrate, but also that doing so would not harm the active circuit elements formed in the semiconductor wafer either at the time of the electroplating operation or during subsequent processing.

The Examiner is right in that a basic metal layer is formed first in the method as claimed such that further copper is electroplated on this basic metal layer. This basic metal layer serves to create a conductive layer for enabling the electroplating of copper on the semiconductor device (page 20, 3rd paragraph in the clean copy of the substitute specification). This basic metal layer is very thin, though, *e.g.* 0.02 μm to 0.3 μm, and hence transparent. It is preferably produced by physical metal deposition and/or by CVD and/or by PECVD. Therefore this layer is not at all a dense layer so that contact of the electroplated copper with the semiconductor wafer substrate is not at all impeded. In fact this layer enables access of the copper layer to the silicon wafer surface so that contamination of the wafer with iron would be very likely if such iron is co-

deposited in the copper layer. This basic layer is usually formed by metal islands deposited on the substrate which are more or less interconnected to each other but which leave much free space between them.

Even the diffusion barrier of, for example, tantalum nitride which may be generated on the silicon wafer prior to the formation of the basic metal layer, has been optimised for inhibiting diffusion of copper into the silicon wafer, and might not completely seal the wafer from the exterior with respect to species other than copper, such that extremely small concentrations of iron (*e.g.* 10^{10} Fe atoms cm^{-3}) might eventually build up in the silicon material due to penetration through this layer. As is described in the paragraph bridging pages 9 and 10 in the clean copy of the substitute specification, copper electroplating would indeed result in iron co-deposition if same would be performed under the conditions which usually prevail during printed circuit boards manufacturing. The barrier layer has been optimised for keeping copper from diffusing therethrough and into the silicon wafer. Given the generally unpredictable nature of the chemical arts, those of ordinary skill in the art could not, based upon the teachings of the prior art, conclude that the barrier layer could act as an effective barrier to the diffusion of iron. Those of ordinary skill in the art would have regarded the chance of having a complete seal of the silicon wafer from iron diffusing through this barrier layer as being very small, given that even five times thicker plated metal layers having a thickness of 1 μm for example do not completely seal from iron diffusing therethrough.

The problem of iron diffusion would be even more acute when one considers the processing steps to which a semiconductor wafer is subjected subsequent to the step of being plated with a copper layer. One has to take into account that annealing steps have to be performed after copper has been deposited onto the wafer. It is well known that under elevated

temperature iron that would be contained in the deposited copper could even more easily diffuse into the wafer through this layer, *e.g.* along any dislocations, grain boundaries etc. in the layer. Diffusivities of copper and iron ions in the layer are of course different so that iron ions may much more easily diffuse through such a barrier than do copper ions. Therefore, contamination by the extremely small concentrations of iron that would be required to exceed the maximum tolerable limits for iron contamination would have to be considered as a very real possibility if the wafer is immersed in an iron containing electroplating bath. Considering that the maximum tolerable limit for the concentration of iron atoms on silicon surfaces was $9 \cdot 10^8$ atoms cm^{-3} for 1999 and is $2.5 \cdot 10^8$ atoms cm^{-3} for 2005 (Table 82a), it can readily be seen that those of ordinary skill in the art would never deliberately expose even silicon wafers having a conductive base coat to electroplating baths containing significant amounts of iron ions.

It has further to be taken into account that the silicon wafer is at an advanced stage of manufacture with respect to the formation therein of integrated circuit components and represents an investment of several tens of thousands of dollars when it is to be coated with copper for the wiring layer. At this stage, given the very high cost of failure, those of ordinary skill in the art would not risk a costly failure by placing the wafer in a liquid bath containing a known detrimental contaminant like iron.

Therefore, at the time the invention was made, those of ordinary skill in the art would not have accepted the presence of iron in the copper layer and for that reason the presence of iron in a copper plating liquid for use in semiconductor device manufacturing had never been considered as a viable alternative until the present invention was made by the applicants.

Not until the applicants proved that iron-containing electroplating solutions could be used to deposit copper layers without any detectable amount of co-deposited iron, would those of

ordinary skill in the art have considered using iron-containing electroplating solutions to electroplate copper onto semiconductor wafers. Exhibit E shows the purity of the copper layer deposited by applicants using the claimed method, and Exhibit E shows that the iron contamination of the copper layer was at most below detectable levels. This result was very surprising since such co-deposition was expected in any case as is described in the paragraph bridging pages 9 and 10 in the clean copy of the substitute specification.

For the reasons presented above, those of ordinary skill in the art would not have looked to the methods for copper plating PCBs as exemplified by the method of DE '231 or the method of Schumacher et al. to provide a solution for copper plating semiconductor wafers, because these methods exclusively relate to PCB manufacturing, which has vastly different requirements for iron contamination as compared to semiconductor wafer manufacturing.

Furthermore, given the state of the art at the time the invention was made, the combination of references applied by the Examiner fails to provide the required motivation to combine the teachings of the references as urged by the Examiner without improper hindsight reconstruction guided by the applicant's own disclosure. Therefore, the combination of references applied by the Examiner fails to establish a *prima facie* case of obviousness. Accordingly, the applicant respectfully submits that the rejections of the claims in the present application as obvious are improper and should be withdrawn. The applicant respectfully further submits that the present application is in condition for allowance and a notice to that effect is earnestly solicited.

If in the Examiner's opinion that is not the case, the Applicant asks that the Examiner kindly contact the undersigned by telephone in an effort to resolve any outstanding issues as expeditiously as possible.

Respectfully submitted,

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